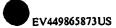## REMARKS

The application has been reviewed in light of the Office Action mailed April 14, 2004. At the time of the Office Action, Claims 1-20 are pending in this application. Claims 1-20 were rejected.

Rejections under 35 U.S.C. § 103(a)

Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,145,049 to David Wong (hereinafter "Wong") in view of U.S. Pat. No. 6,205,467 to Lambrecht et al. (hereinafter "Lambrecht"). Applicants respectfully traverse the rejections and submit that the references relied upon do not teach or suggest, individually or in combination, what is being claimed.

The present invention simultaneously transfers data contained in an array of source registers to an array of destination (shadow) registers based upon a single processor instruction that may be executed within one processor cycle. In addition, the invention can simultaneously transfer the data in the array of destination (shadow) registers to the array of source registers based upon another single processor instruction that also may be executed within one processor cycle. Once the transfer data array instruction is executed by the processor, the invention simultaneously transfers the data between the array of registers without involvement of the processor. This allows the processor to execute subsequent program instructions without being burdened by having to control the transfer of data contained in a plurality of registers to another plurality of registers, and this data transfer may be performed before the next processor program instruction is executed. These array data transfer instructions may be performed for either interrupt or non-interrupt program processing.

In contrast, Wong teaches a shadow register set that is merely additional cache memory associated with the processor. During processing in the Wong invention, floating point data is stored in memory and in the shadow registers. The memory and shadow register store operations are monitored (snooped) and if the main memory location has not been changed from what was written to the corresponding shadow register, the processor will use the data stored in the shadow register instead of requiring the more time consuming operation of getting the data from main memory. This is a cache type operation and requires processor intervention to obtain data from a plurality of memory locations (array of registers). The Wong invention is directed toward context switching between floating point and multimedia data processing of floating point data.

Lambrecht teaches a microprocessor having a context save unit that periodically performs context saves into a context storage location. The context save unit is configured to perform a context save at the occurrence of a variety of events. The execution units of the microprocessor do not initiate the context save, only the context save unit initiates the context save. The microprocessor utilizes the context save after an interrupt, if appropriate (the context saves are asynchronous to the execution unit program and interrupt instruction operation). The Lambrecht invention uses multiple cache write operations during a context save, wherein context data is saved into one cache memory location at a time, and takes longer than a single execution unit (processor) cycle time. The present invention performs a data transfer from an array (plurality) of primary registers to an array (plurality) of shadow registers, simultaneously and within one processor cycle.

Applicants respectfully submit that the references relied upon do not teach or suggest, individually or in combination, a shadow register array control instruction executed by a

processor that initiates a transfer of data from a source array of registers to a destination array of registers within one processor cycle as recited in independent claims 1 and 11. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. In addition, the suggested combination could not be achieved without significant structural modification of either reference since there is no teachings or suggestion of an array of source registers and an array of destination registers wherein data may be transferred therebetween within one processor cycle.

Claims 2-10 depend from independent claim 1 and claims 12-20 depend from independent claim 11, and contain all limitations thereof.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicants reserve the right to subsequently take up prosecution on the claims as originally filed in this or appropriate continuation, continuation-in-part and/or divisional applications.

Applicants respectfully request that the amendments submitted herein be entered, and further request reconsideration in light of the amendments and remarks contained herein.

Applicants respectfully request withdrawal of all objections and rejections, and that there be an early notice of allowance.

SUMMARY

In light of the above amendments and remarks Applicants respectfully submit that the application is now in condition for allowance and early notice of the same is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicants believes that there are no fees due in association with the filing of this Response. However, should the Commissioner deem that any fees are due, including any fees for extensions of time, Applicants respectfully request that the Commissioner accept this as a Petition Therefor, and direct that any and all fees due are charged to Baker Botts L.L.P. **Deposit Account No. 02-0383**, *(formerly Baker & Botts, L.L.P.)* **Order Number 068354.1441.**

Respectfully submitted,

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